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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
BREWSTER, WILLIAM M	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 12/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/619,114	SHEU ET AL.	
	Examiner	Art Unit	
	William M. Brewster	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 November 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *26-45* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *26-45* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 26-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Puchner et al., U.S. Patent No. 6,342,429 B1 in view of Noble, U.S. Patent No. 5,726,095.

Puchner teaches an NMOS transistor having an improved narrow width Vt roll-off comprising:

(a) in fig. 2B, a substrate 200 that includes shallow trench isolation (STI) features which are comprised of a shallow trench 206 with sloped sidewalls and a bottom, in fig. 2C, an oxide liner 202 formed on said shallow trench sidewalls and bottom, and in fig. 2E, an insulator layer 220 formed on said oxide liner that fills said shallow trench and extends to a level that is above the top of said substrate, col. 4, lines 22-42;

limitations from claim 28: the NMOS transistor of claim 26 wherein the depth of said shallow trench is about 1500 to 5000 Angstroms: 0.05 - 0.5 μm, col. 3, lines 38 - 62;

limitations from claim 29: the NMOS transistor of claim 26 wherein said oxide liner has a thickness of about 50 to 300 Angstroms: 50-500 Å;

(b) in fig. 2D, an active area formed between two adjacent shallow trenches in said substrate; said active area having an indium doped region that is adjacent to top comers of said shallow trenches, col. 3, line 62 - col. 4, line 9, wherein in the trench 206 has sloping sidewalls which when implanted with indium, some ions are implanted on the edges of the sidewall adjacent to the top corners of said shallow trenches;

(c) a gate dielectric layer 202 formed on said active area;

limitations from claim 27: in fig. 3, the NMOS transistor wherein said substrate is also comprised of a second p-type dopant in said active areas: boron, col. 4, line 56 - col. 5, line 5.

Puchner does not teach the extension of the gate layer, but Noble does. Noble teaches in fig. 3L-3M, an NMOS with a substrate 12, shallow trenches 14, an oxide 26', and (d) a patterned gate layer 16 formed on said fate dielectric layer wherein said gate layer extends over said adjacent shallow trenches, col. 6, lines 14-50;

limitations from claims 30, 33: the NMOS structure, wherein said insulator layer is comprised of SiO_2 or a low k dielectric material; wherein said gate dielectric layer is comprised of SiO_2 or an upper high k dielectric metal oxide layer on a lower interfacial layer: SiO_2, layer 26', col. 6, lines 14-27;

limitations from claim 35: the NMOS structure wherein said gate layer 16 is comprised of doped polysilicon, among others, tungsten, col. 6, lines 14-37.

Noble gives motivation in col. 1, lines 46-60. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to recognize that combining

Noble's process with Puchner's invention would have been beneficial because it helps control parasitic voltage threshold.

Neither Puchner nor Noble specify for claims 28, the width of the shallow trench, in claim 31, the concentration of the indium, and the thickness of the indium range, for claim 32, the distance of extension of the indium region, and for claim 34, the thickness of the gate layer. However, the practitioner may optimize these dimensions.

"Normally, it is to be expected that a change in temperature, or in concentration, or in both, would be an unpatentable modification. Under some circumstances, however, changes such as these may impart patentability to a process if the particular ranges claimed produce a new and unexpected result which is different in kind and not merely degree from the results of the prior art . . . such ranges are termed 'critical ranges' and the applicant has the burden of proving such criticality . . . More particularly, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation."

In re Aller 105 USPQ 233, 255 (CCPA 1955). See also In re Waite 77 USPQ 586 (CCPA 1948); In re Scherl 70 USPQ 204 (CCPA 1946); In re Irmscher 66 USPQ 314 (CCPA 1945); In re Norman 66 USPQ 308 (CCPA 1945); In re Swenson 56 USPQ 372 (CCPA 1942); In re Sola 25 USPQ 433 (CCPA 1935); In re Dreyfus 24 USPQ 52 (CCPA 1934).

Note that the specification contains no disclosure of either the critical nature of the claimed dimensions of any unexpected results arising there from. Where patentability is aid to be based upon particular chosen dimensions or upon another variable recited in a

claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Claim 36 is rejected under 35 U.S.C. 103(a) as being unpatentable over Puchner in view of Noble as applied to claims 25-35 above, and further in view of Eklund et al., U.S. Publication No. 2003/0096466 A1.

Neither Puchner nor Noble teaches a gate layer of amorphous silicon, but Eklund does. Eklund teaches in fig. 1F, substrate 12, shallow trenches 30, NMOS with gate oxides 50, and gate layer 60, p. 2, ¶ 21-22, wherein said gate layer is comprised of undoped polysilicon or amorphous silicon. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to recognize that combining Eklund's process with Puchner's or Noble's invention would have been beneficial because Eklund's process enables the practitioner more options for gate formation including skipping thermal annealing for crystallization.

Claims 37-45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Puchner in view of Noble.

Puchner teaches an NMOS transistor having an improved narrow width Vt roll-off comprising:

(a) in fig. 2B, a substrate 200 that includes shallow trench isolation (STI) features which are comprised of a shallow trench 206 with sloped sidewalls and a bottom, in fig. 2C, an oxide liner 202 formed on said shallow trench sidewalls and bottom, and in fig. 2E, an

insulator layer 220 formed on said oxide liner that fills said shallow trench and extends to a level that is above the top of said substrate, col. 4, lines 22-42;

limitations from claim 39: the NMOS transistor of claim 26 wherein the depth of said shallow trench is about 1500 to 5000 Angstroms: 0.05 - 0.5 μm, col. 3, lines 38 - 62;

limitations from claim 40: the NMOS transistor of claim 26 wherein said oxide liner has a thickness of about 50 to 300 Angstroms: 50-500 Å;

(b) in fig. 2D, an active area formed between two adjacent shallow trenches in said substrate; said active area having an indium doped region that is adjacent to top comers of said shallow trenches, col. 3, line 62 - col. 4, line 9, wherein in the trench 206 has sloping sidewalls which when implanted with indium, some ions are implanted on the edges of the sidewall adjacent to the top corners of said shallow trenches;

(c) a gate dielectric layer 202 formed on said active area;

limitations from claim 38: in fig. 3, the NMOS transistor wherein said substrate is also comprised of a second p-type dopant in said active areas: boron, col. 4, line 56 - col. 5, line 5.

Puchner does not teach the extension of the gate layer, but Noble does. Noble teaches in fig. 3L-3M, an NMOS with a substrate 12, shallow trenches 14, an oxide 26', and (d) a patterned gate layer 16 formed on said fate dielectric layer wherein said gate layer extends over said adjacent shallow trenches, col. 6, lines 14-50;

limitations from claims 41, 44: the NMOS structure, wherein said insulator layer is comprised of SiO_2 or a low k dielectric material; wherein said gate dielectric layer is comprised of SiO_2 or an upper high k dielectric metal oxide layer on a lower interfacial layer: SiO_2, layer 26', col. 6, lines 14-27.

Noble gives motivation in col. 1, lines 46-60. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to recognize that combining Noble's process with Puchner's invention would have been beneficial because it helps control parasitic voltage threshold.

For limitations of claim 37, the combination of Puchner and Noble would have the limitations of lines 10-12, wherein said active area having an indium doped region that is adjacent to top corner of said shallow trenches and extends under part of the gate dielectric layer. This is due to the Indium implantation of Puchner being driven through the oxide 208 at the corners of the STI trench 206 in fig. 2D. When the subsequent processing of forming the oxide 220, and in Noble: in fig. 3E, the themo-oxide col. 4, lines 27-54, the thermal cycles col. 5, lines 31-45, and the diffusion temperatures and the metallization contacts of col. 6, lines 28-37.

All of these thermal cycles diffuse the indium from the silicon below the corners of the STI to extend underneath the gate dielectric layer. Proffered as evidence of diffusion is Wolf, V. I, pp. 251-61. on p. 250, the diffusion equation is listed in equation 30 in which diffusion is dependent on Temperature. With the thermal cycles listed above, the Indium will diffuse to extend underneath the gate layer in the device according to the diffusion equation in the elevated temperature cycles.

Neither Puchner nor Noble specify for claims 39, the width of the shallow trench, in claim 42, the concentration of the indium, and the thickness of the indium range, for claim 43, the distance of extension of the indium region, and for claim 45, the thickness of the gate layer. However, the practitioner may optimize these dimensions.

"Normally, it is to be expected that a change in temperature, or in concentration, or in both, would be an unpatentable modification. Under some circumstances, however, changes such as these may impart patentability to a process if the particular ranges claimed produce a new and unexpected result which is different in kind and not merely degree from the results of the prior art . . . such ranges are termed 'critical ranges' and the applicant has the burden of proving such criticality . . . More particularly, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation."

In re Aller 105 USPQ 233, 255 (CCPA 1955). See also In re Waite 77 USPQ 586 (CCPA 1948); In re Scherl 70 USPQ 204 (CCPA 1946); In re Irmscher 66 USPQ 314 (CCPA 1945); In re Norman 66 USPQ 308 (CCPA 1945); In re Swenson 56 USPQ 372 (CCPA 1942); In re Sola 25 USPQ 433 (CCPA 1935); In re Dreyfus 24 USPQ 52 (CCPA 1934).

Note that the specification contains no disclosure of either the critical nature of the claimed dimensions of any unexpected results arising there from. Where patentability is aid to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Response to Arguments

Applicant's arguments filed 24 November 2004 have been fully considered but they are not persuasive. Applicant argues that the Indium is doped at the bottom of the trench and is not present at the corners.

Examiner respectfully disagrees. While examiner stipulates that the majority of Indium would be implanted in the bottom, some still resides at the corners. In fig. 2D, the trench 206, is not a rectilinear box shape, but curved, leaving silicon substrate material at the corners to be implanted by the Indium which is self-aligned to implant in the regions not covered by the Nitride 204. For further evidence, fig. 3 displays an Indium concentration in different parts of the targeted silicon.

For claims 37-45, the diffusion of Indium is explained above.

Examiner must give claims their broadest reasonable interpretation, MPEP §2111, "During patent examination, the pending claims must be 'given the broadest reasonable interpretation consistent with the specification.' Applicant always has the opportunity to amend the claims during prosecution and broad interpretation by the examiner reduces the possibility that the claim, once issued, will be interpreted more broadly than is justified, *In re Pratter*, 415 F.2d 1393, 1404-05, 162 USPQ 541, 550-51 (CCPA 1969), *In re Morris*, 127 F.3d 1048, 1054-55, 44 USPQ2d 1023, 1027-28 (Fed. Cir. 1997)." Also see *In re Zletz*, 13 USPQ 2d. 1320 (Fed. Cir. 1989).

For the above reasons, the rejection is deemed proper.

Conclusion

For claims 26-36:

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

For claims 37-45:

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to William M. Brewster whose telephone number is 571-272-1854. The examiner can normally be reached on Full Time.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 571-272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

16 December 2004
WB

OLIK CHAUDHURI
SUPERVISORY PATENT EXAMINER
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